Exhibit A

Glenn D Reinman

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Research Interests

Computer architecture, augmented reality, parallel programming, compiler optimizations, and systems.

Education

- **University of California - San Diego (San Diego, CA)**
  - Doctor of Philosophy degree in Computer Science, June 2001
    Advisor: Professor Brad Calder.
  - Master of Science degree in Computer Science, March 1999.
- **Massachusetts Institute of Technology (Cambridge, MA)**
  - Bachelor of Science degree in Computer Science and Engineering, June 1996.

Recent Research Highlights

- **Accelerator-Rich Chip Multiprocessors (CMPs)** – energy-efficient high-performance SoC platforms that features both application-specific accelerators and heterogeneous cores.
- **RF Interconnect** – a promising alternative interconnect for both on-chip and off-chip communication for future CMPs. It can be adaptively tuned to the communication needs of an individual application. We have also explored wireless RF interconnect and RF-integrated memory technology.
- **Mobile Augmented Reality** – sensing and guidance framework for real-time critical situations. We are leveraging our work on automated planning engines and our work to accelerate computer vision as the basis for this line of research.
- **Real-Time Physics** – we have proposed a novel physics processor and explored dynamically trading accuracy for improved performance while maintaining believability.
- **Dynamically Leveraging Statically Partitioned Resources** – CMPs statically partition resources for scalability and performance/energy efficiency. We look at dynamically composing these static resources into more powerful components.

Work Experience

- **University of California – Los Angeles (Los Angeles, CA)**
  - Assistant Professor (2001-2007)
  - Associate Professor (2007-Present)
- **Expert Witness Testimony**
  - Served as an expert witness for ten independent patent infringement cases. Have been deposed, written detailed expert reports, constructed patent claim charts, deciphered decades-old designs from schematics and microcode, uncovered prior work to anticipate claims, architecturally simulated patented designs to demonstrate claim validity, and worked closely with lawyers to educate them on technical details.
- **University of California - San Diego, Research Assistant (San Diego, CA)**
  - Implemented a profile-based approach to classifying loads for memory renaming, value prediction, and dependence prediction using SimpleScalar and ATOM. Created an aggressive fetch unit using a two-level branch prediction structure called an FTB. Worked with SimpleScalar to implement a hybrid load prediction mechanism, combining renaming, value prediction, address prediction, and dependence prediction. Explored importance of confidence in value prediction. Used C and C++. (Fall 1997-Spring 2001)
  - Implemented a contention resolution scheme for embarassingly parallel applications (such as the DOT project at the San Diego Supercomputing Center). Worked in MPICH and C. (Spring 1997-Fall 1997)

- **COMPAQ (**now **HP) - Western Research Lab, Summer Internship 1999 (Palo Alto, CA)**
  Expanded the CACTI cache compiler (CACTI 2.0). Enhancements include fully associative cache model, power modeling, multiple port models, transistor tuning, and tag path balancing.
- **Intel Corporation - Microprocessor Research Lab, Summer Intern 1998 (Hillsboro, OR)**
  Studied the viability of caching state from the branch predictor, TLB, and BTB in the second level data cache. Modified SimpleScalar to use ITR traces for Win95 applications for initial predictability experiments. Used out-of-order simulation with SimpleScalar to determine the effectiveness of this technique.

Teaching Experience

- **University of California – Los Angeles, Assistant Professor (Los Angeles, CA)**
  - ***Computer Systems Architecture*** (CSM151B - Upper Division Undergraduate class) - I have taught this class since Winter 2003, covering instruction set architecture design, ALU design, processor datapath and control design, pipelining, caches, virtual memory, IO devices, multithreading, multiprocessors, and multicore architectures.
  - ***Advanced Topics in Microprocessor Design*** (CS259 - Graduate class) - I introduced this class in Spring 2002, covering cutting edge research in general purpose microarchitecture. The processor pipeline is explored in detail, with attention to performance, complexity, cycle time, power, and area. Recent real world architectures are used for illustration, along with on-going research efforts in topics that includes multicore processors, NoC design, cache coherence mechanisms, GPU design and programming, branch prediction, load speculation, simultaneous multithreading, cache design/prefetching, register file design, and various techniques to combat processor scaling trends. Introduction to cycle-accurate microprocessor simulation. Lab intensive class designed to give students practical experience with simulation techniques and tricks. On-going work in architecture and compilers is discussed during class and then integrated into lab assignments using the simulation infrastructure.
  - ***Microprocessor Simulation*** (CS259 - Graduate class) - I introduced this class in Winter 2003, providing a practical application of my Advanced Topics class students make use of execution-driven cycle-accurate processor simulators.
  - ***Parallel and Distributed Systems*** (CS133 - Upper Division Undergraduate class) - I have completely reorganized this class in Winter 2007 to focus on programming in OpenMP, POSIX threads, MPI, and CUDA for both shared and distributed memory multiprocessors. The class also has a component on next generation chip multiprocessors, including design tradeoffs and un-core optimizations.
  - ***Computer Organization*** (CS33 - Lower Division Undergraduate class) - I completely reorganized this class in Fall 2009 to make it a gateway systems class using low-level C programming and x86 assembly. It is a practical class, with several labs including an introduction to parallel programming with CUDA as the demonstration vehicle.
  - ***Computer Science Seminar Series*** (CS201 - Graduate class)
- **University of California - San Diego, Teaching Assistant (San Diego, CA)**
  - Teaching Assistant - taught discussion sections for classes on data structures, artificial intelligence, and compilers. Recipient of 1996/97 TA Excellence Award.

Publications

Refereed Conference and Workshop Publications:

1. Yu-Ting Chen, Jason Cong, Hui Huang, Chunyue Liu, Raghu Prabhakar and Glenn Reinman. Static and Dynamic Co-Optimizations for Blocks Mapping in Hybrid Caches. *International Symposium on Low Power Electronics and Design (ISLPED)*, Jul/Aug 2012.
2. Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Beayna Grigorian and Glenn Reinman. CHARM: A Composable Heterogeneous Accelerator-Rich Microprocessor. *International Symposium on Low Power Electronics and Design (ISLPED)*, Jul/Aug 2012.
3. Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Chunyue Liu and Glenn Reinman. BiN: A Buffer-in-NUCA Scheme for Accelerator-Rich CMPs. *International Symposium on Low Power Electronics and Design (ISLPED)*, Jul/Aug 2012.

4. Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Beayna Grigorian, and Glenn Reinman. TBD. *Dark Silicon Workshop (DaSi - held in conjunction with ISCA)*, Jun 2012
5. Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Beayna Grigorian, and Glenn Reinman. Architecture Support for Accelerator-Rich CMPs. *Design Automation Conference (DAC)*, Jun 2012
6. Yu-Ting Chen, Jason Cong, Hui Huang, Bin Liu, Chunyue Liu, Miodrag Potkonjak and Glenn Reinman. Dynamically Reconfigurable Hybrid Cache: An Energy-Efficient Last-Level Cache Design. *Conference on Design, Automation, and Test in Europe (DATE)*, Mar 2012.
7. Yangkyo Kim, Gyungsu Byun, Adrian Tang, Jason Cong, Glenn Reinman, and M. F. Chang. An 8Gb/s/pin 4pJ/b/pin Single-T-Line Dual (Base+RF) Band Simulataneous Bidirectional Mobile Memory I/O Interface with Inter-Channel Interference Suppression. *International Solid-State Circuits Conference (ISSCC)*, Feb 2012.
8. Jason Cong, Mohammad Ali Ghodrat, Michael Gill, Hui Huang, Bin Liu, Raghu Prabhakar, Glenn Reinman, and Marco Vitanza. Compilation and Architecture Support for Customized Vector Instruction Extension. *Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jan/Feb 2012.
9. Mubbasir Kapadia, Matthew Wang, Glenn Reinman, and Petros Faloutsos. Improved Benchmarking for Crowd Simulations. *Motion In Games (MIG)*, Nov 2011
10. Kanit Therdsteerasukdi, Gyungsu Byun, Jeremy Ir, Glenn Reinman, Jason Cong, and Frank Chang. The DIMM Tree Architecture: A High Bandwidth and Scalable Memory System. *IEEE International Conference on Computer Design (ICCD),* Oct 2011.
11. Yu-Ting Chen, Jason Cong and Glenn Reinman. HC-Sim: A Fast and Exact L1 Cache Simulator with Scratchpad Memory Co-simulation Support. *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)*, Oct 2011.
12. Beayna Grigorian, Marco Vitanza, Jason Cong, and Glenn Reinman. Accelerating Vision and Navigation Applications on a Customizable Platform. *International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, Sep 2011.
13. Mubbasir Kapadia, Matthew Wang, Shawn Singh, Glenn Reinman, and Petros Faloutsos. Scenario Space: Characterizing Coverage, Quality, and Failure of Steering Algorithms. *Symposium on Computer Animation (SCA)*, Aug 2011.
14. Jason Cong, Karthik Gururaj, Hui Huang, Chunyue Liu, Glenn Reinman and Yi Zou. An Energy-Efficient Adaptive Hybrid Cache. *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug 2011.
15. Mubbasir Kapadia, Shawn Singh, Glenn Reinman, and Petros Faloutsos. Multi-Actor Planning for Directable Simulations. *Workshop on Digital Media and Digital Content Management*, May 2011.
16. Gyungsu Byun, Yangkyo Kim, Jongsun Kim, Sai-Wang Tam, Jason Cong, Glenn Reinman, and M. F. Chang. An 8.4Gb/s 2.5pJ/b Mobile Memory I/O Interface Using Bi-directional and Simultaneous Dual (Base+RF)-Band Signaling. *International Solid-State Circuits Conference (ISSCC)*, Feb 2011.
17. Jason Cong, Mohammadali Ghodrat, Michael Gill, Chunyue Liu, Glenn Reinman and Yi Zou. AXR-CMP: Architecture Support in Accelerator-Rich CMPs. *Workshop on SoC Architecture, Accelerators and Workloads (SAW-2)*, Feb 2011.
18. Shawn Singh, Mubbasir Kapadia, Billy Hewlett, Glenn Reinman and Petros Faloutsos. A Modular Framework for Adaptive Agent-Based Steering. *Symposium on Interactive 3D Graphics and Games (I3D)*, Feb 2011.
19. Zoran Budimli□ , Alex Bui, Jason Cong, Glenn Reinman, Vivek Sarkar. Modeling and Mapping for Customizable Domain-Specific Computing. Workshop on Concurrency for the Application Programmer (CAP), co-located with SPLASH 2010, Oct 2010.
20. Jason Cong, Chunyue Liu, and Glenn Reinman. ACES: Application-specific cycle elimination and splitting for deadlock-free routing on irregular network-on-chip. *Design Automation Conference (DAC)*, Jun 2010.
21. Shawn Singh, Mubbasir Kapadia, Petros Faloutsos, and Glenn Reinman. On the Interface Between Steering and Animation for Autonomous Characters. *Workshop on Crowd Simulation held in conjunction with the 23rd Annual Conference on Computer Animation and Social Agents*, May 2010.
22. Shawn Singh, Mubbasir Kapadia, Glenn Reinman and Petros Faloutsos. An Open Framework for Developing, Evaluating, and Sharing Steering Algorithms. *Motion In Games (MIG)*, Nov 2009.

23. Suk-Bok Lee, Sai-Wang Tam, Ioannis Pefkianakis, Songwu Lu, M. Frank Chang, Chuanxiong Guo, Glenn Reinman, Chunyi Peng, Mishali Naik, Lixia Zhang, and Jason Cong. A Scalable Micro Wireless Interconnect Structure for CMPs. *International Conference on Mobile Computing and Networking*, Sept 2009.
24. Mubbasir Kapadia, Shawn Singh, Brian Allen, Glenn Reinman, and Petros Faloutsos. An Interactive Framework for Specifying and Detecting Steering Behaviors. *Symposium on Computer Animation (SCA)*, Aug 2009.
25. Jason Cong, M. Frank Chang, Glenn Reinman, and Sai-Wang Tam, Multiband RF-Interconnect for Reconfigurable Network-on-Chip Communications, *System Level Interconnect Prediction (SLIP 2009)*, July 2009.
26. M. Frank Chang, Jason Cong, Adam Kaplan, Mishali Naik, Jagannath Premkumar, Glenn Reinman, Eran Socher, and Sai-Wang Tam. Power Redu ction of CMP Communication Networks via RF-Interconnects. *International Symposium on Microarchitecture (MICRO)*, Nov 2008.
27. Jason Cong, Karthik Gururaj, Guoling Han, Adam Kaplan, Mishali Naik, and Glenn Reinman. MC-Sim: An Efficient Simulation Tool for MPSoC Designs. *International Conference on Computer-Aided Design (ICCAD)*, Nov 2008.
28. Shawn Singh, Mubbasir Kapadia, Mishali Naik, Petros Faloutsos, and Glenn Reinman. Watch Out! A Framework for Evaluating Steering Behaviors. *Proceedings of Motion In Games (MIG)*, June 2008.
29. M. Frank Chang, Eran Socher, Sai-Wang Tam, Jason Cong, and Glenn Reinman. RF Interconnects for Communications On-Chip. *International Symposium on Physical Design (ISPD)*, Apr 2008.
30. M. Frank Chang, Jason Cong, Adam Kaplan, Mishali Naik, Glenn Reinman, Eran Socher, and Sai-Wang Tam. CMP Network-on-Chip Overlaid With Multi-Band RF-Interconnect. *International Symposium on High-Performance Computer Architecture (HPCA)*, Feb 2008. **BEST PAPER AWARD**
31. Tom Yeh, Petros Faloutsos, Sanjay Patel, Milos Ercegovac, and Glenn Reinman. The Art of Deception: Adaptive Precision Reduction for Area Efficient Physics Acceleration. *International Symposium on Microarchitecture (MICRO)*, Dec 2007.
32. Yongxiang Liu, Yuchun Ma, Eren Kursun, Jason Cong, and Glenn Reinman. Fine Grain 3D Integration for Microarchitecture Design Through Cube Packing Exploration. *IEEE International Conference on Computer Design (ICCD)*, Oct 2007.
33. Yongxiang Liu, Yuchun Ma, Eren Kursun, Jason Cong, and Glenn Reinman. 3D Architecture Modeling and Exploration. *VLSI/ULSI Multilevel Interconnection Conference*, Sept 2007.
34. Tom Yeh, Petros Faloutsos, Sanjay Patel, and Glenn Reinman. ParallAX: An Architecture for Real-Time Physics. In *34th Annual International Symposium on Computer Architecture (ISCA),* June 2007
35. Yuchun Ma, Zhuoyuan Li, Jason Cong, Xianlong Hong, Glenn Reinman, Sheqin Dong, and Qian Zhou. Micro-architecture Pipelining Optimization with Throughput-Aware Floorplanning. *12th Asia and South Pacific Design Automation Conference (ASPDAC)*, Jan 2007.
36. Vasily G. Moshnyaga, Hua Vo, Glenn Reinman, and Miodrag Potkonjak. Reducing Energy of DRAM/Flash Memory System by OS-Controlled Data Refresh. In *International Symposium on Circuits and Systems (ISCAS)*, May 2007.
37. Anahita Shayesteh, Glenn Reinman, Norm Jouppi, Suleyman Sair, and Tim Sherwood. Improving the Performance and Power Efficiency of Shared Helpers in CMPs. *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES),* Oct 2006.
38. Vasily Moshnyaga, Hoa Vo, Glenn Reinman, and Miodrag Potkonjak. Handheld System Energy Reduction by OS-Driven Refresh. *Power and Timing Modeling, Optimization, and Simulation (PATMOS)*, September 2006.
39. Tom Yeh, Petros Faloutsos, and Glenn Reinman. Enabling Real-Time Physics Simulation in Future Interactive Entertainment. *ACM SIGGRAPH Video Game Symposium*, Aug 2006.
40. Jason Cong, Ashok Jagannathan, Yuchun Ma, Glenn Reinman, Jie Wei, and Yan Zhang. An Automated Design Flow for 3D Microarchitecture Evaluation. *11th Asia and South Pacific Design Automation Conference (ASPDAC)*, Jan 2006.
41. Anahita Shayesteh, Eren Kursun, Tim Sherwood, Suleyman Sair, and Glenn Reinman. Reducing the Latency and Area Cost of Core Swapping through Shared Helper Engines. *IEEE International Conference on Computer Design (ICCD),* Oct 2005.

42. Yongxiang Liu, Gokhan Memik, and Glenn Reinman. Reducing the Energy of Speculative Instruction Schedulers. *IEEE International Conference on Computer Design (ICCD),* Oct 2005.
43. Tom Yeh and Glenn Reinman. Fast and Fair: Data-stream Quality of Service. *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES),* Sep 2005.
44. Jason Cong, Ashok Jagannathan, Glenn Reinman, and Yuval Tamir. Understanding The Energy Efficiency of SMT and CMP with Multi-clustering. *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, Aug 2005.
45. Yongxiang Liu, Anahita Shayesteh, Gokhan Memik, and Glenn Reinman. Tornado Warning: the Perils of Selective Replay in Multithreaded Processors. *International Conference on Supercomputing (ICS)*, June 2005.
46. Jason Cong, Yiping Fan, Guoling Han, Ashok Jagannathan, Glenn Reinman, and Zhiru Zhang. Instruction Set Extension with Shadow Registers for Configurable Processors. *13th ACM International Symposium on Field-Programmable Gate Arrays,* Feb 2005.
47. Ashok Jagannathan, Hannah Honghua Yang, Kris Konigsfeld, Dan Milliron, Mosur Mohan, Michail Romesis, Glenn Reinman, and Jason Cong. Microarchitecture Evaluation with Floorplanning and Interconnect Pipelining. *Asia South Pacific Design Automation Conference (ASPDAC)*, Jan 2005.
48. Eren Kursun, Glenn Reinman, Suleyman Sair, Anahita Shayesteh, and Tim Sherwood. Low-Overhead Core Swapping for Thermal Management. *Workshop on Power-Aware Computer Systems (PACS'04) held in conjunction with the 37th Annual International Symposium on Microarchitecture*, December 2004.
49. Yongxiang Liu, Anahita Shayesteh, Gokhan Memik, and Glenn Reinman. The Calm Before the Storm: Reducing Replays in the Cyclone Scheduler. *IBM T.J. Watson Conference on Interaction between Architecture, Circuits, and Compilers,* Oct 2004.
50. Jason Cong, Ashok Jagannathan, Glenn Reinman, and Yuval Tamir. A Communication-Centric Approach to Instruction Steering for Future Clustered Processors. *IBM T.J. Watson Conference on Interaction between Architecture, Circuits, and Compilers,* Oct 2004.
51. Yongxiang Liu, Anahita Shayesteh, Gokhan Memik, and Glenn Reinman. Scaling the Issue Window with Look-Ahead Latency Prediction. *International Conference on Supercomputing (ICS)*, June 2004.
52. Fang-Chung Chen, Foad Dabiri, Roozbeh Jafari, Eren Kursun, Vijay Raghunathan, Thomas Schoellhammer, Doug Sievers, Deborah Estrin, Glenn Reinman, Majid Sarrafzadeh, Mani Srivastava, Ben Wu, Yang Yang. Reconfigurable Fabric: An enabling technology for pervasive medical monitoring. *Communication Networks and Distributed Systems Modeling and Simulation Conference*, Jan 2004.
53. Jason Cong, Ashok Jagannathan, Glenn Reinman, and Michail Romesis. Microarchitecture Evaluation with Physical Planning. *Design Automation Conference (DAC)*, 2003.
54. Gokhan Memik, Glenn Reinman, and William H. Mangione-Smith. Reducing Energy and Delay Using Efficient Victim Caches. *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2003.
55. Gokhan Memik, Glenn Reinman, and William H. Mangione-Smith. Just Say No: Benefits of Early Cache Miss Determination. *In the proceedings of the 9th IEEE/ACM International Symposium on High Performance Computer Architecture (HPCA)*, Feb. 2003.
56. Glenn Reinman, Brad Calder and Todd Austin. High Performance and Energy Efficient Serial Prefetch Architecture. *In the proceedings of the 4th International Symposium on High Performance Computing*, May 2002, (c) Springer-Verlag.
57. Glenn Reinman, Brad Calder, and Todd Austin. Fetch Directed Instruction Prefetching. In *32nd International Symposium on Microarchitecture (MICRO),* November 1999.
58. Glenn Reinman, Brad Calder, Dean Tullsen, Gary Tyson, and Todd Austin. Classifying Load and Store Instructions for Memory Renaming. In *ACM International Conference on Supercomputing (ICS),* June 1999.
59. Glenn Reinman, Todd Austin, and Brad Calder. A Scalable Front-End Architecture for Fast Instruction Delivery. In *26th Annual International Symposium on Computer Architecture (ISCA),* May 1999.
60. Brad Calder, Glenn Reinman, and Dean Tullsen. Selective Value Prediction. In *26th Annual International Symposium on Computer Architecture (ISCA),* May 1999.
61. Glenn Reinman and Brad Calder. Predictive Techniques for Aggressive Load Speculation. In *31st Annual International Symposium on Microarchitecture (MICRO)*, December 1998.

Refereed Journal Publications:

62. Kanit Therdsteerasukdi, Gyung-Su Byun, Jeremy Ir, Glenn Reinman, Jason Cong, and M.F. Chang. Utilizing Radio Frequency Interconnect for a Many-DIMM DRAM System. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* 2012.
63. Mubbasir Kapadia, Shawn Singh, Wiliam Hewlett, Glenn Reinman, and Petros Faloutsos. Parallelized Egocentric Fields for Autonomous Navigation. *The Visual Computer*, 2012.
64. Yanghyo Kim, Sai-Wang Tam, Gyung-Su Byun, Hao Wu, Lan Nan, Glenn Reinman, Jason Cong, and Mau-Chung Frank Chang. Analysis of Non-Coherent ASK Modulation Based RF-Interconnect for Memory Interface. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* Jun 2012.
65. Kanit Therdsteerasukdi, Gyungsu Byun, Jason Cong, Frank Chang, and Glenn Reinman. Utilizing RF-I and Intelligent Scheduling for Better Throughput/Watt in a Mobile GPU Memory System. *ACM Transactions on Architecture and Code Optimization (**TACO**)*, Jan 2012.
66. Mubbasir Kapadia, Shawn Singh, Glenn Reinman, and Petros Faloutsos. A Behavior Authoring Framework for Multi-Actor Simulations. *IEEE Computer Graphics and Applications: Special Issue on Digital Content Authoring*, December 2011
67. Shawn Singh, Mubbasir Kapadia, Glenn Reinman and Petros Faloutsos. Footstep Navigation for Dynamic Crowds. *Computer Animation and Virtual Worlds*, April 2011.
68. Jason Cong, Vivek Sarkar, Glenn Reinman, and Alex Bui. Customizable Domain-Specific Computing. *IEEE Design & Test*, March/April 2011.
69. Tom Yeh, Glenn Reinman, Sanjay Patel, and Petros Faloutsos. Fool me twice: Exploring and exploiting error tolerance in physics-based animation. *ACM Transactions on Graphics (TOG)*, December 2009.
70. Shawn Singh, Mubbasir Kapadia, Petros Faloutsos, and Glenn Reinman. SteerBench: A Benchmark Suite for Evaluating Steering Behaviors. *Journal of Computer Animation and Virtual Worlds*, Feb 2009.
71. Yuchun Ma, Yongxiang Liu, Eren Kursun, Glenn Reinman, and Jason Cong. Investigating the Effects of Fine-Grain Three-Dimensional Integration on Microarchitecture Design. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Oct 2008.
72. Jason Cong, Guoling Han, Ashok Jagannathan, Glenn Reinman, and Krzysztof Rutkowski. Accelerating Sequential Applications on CMPs Using Core Spilling. In *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, August 2007.
73. Glenn Reinman and Gruia Pitigoi-Aron. Trace Cache Miss Tolerance for Deeply Pipelined Superscalar Processors. In *IEE Proceedings on Computers and Digital Techniques,* September 2006.
74. Eren Kursun, Anahita Shayesteh, Suleyman Sair, Tim Sherwood, and Glenn Reinman. An Evaluation of Deeply Decoupled Cores. In the *Journal of Instruction Level Parallelism (JILP)*, February 2006.
75. Anahita Shayesteh, Glenn Reinman, Norm Jouppi, Suleyman Sair, and Tim Sherwood. Dynamically Configurable Shared CMP Helper Engines for Improved Performance. In SIGARCH Computer Architecture News, November 2005.
76. Gokhan Memik, Glenn Reinman, and Bill Mangione-Smith. Precise Instruction Scheduling. In the *Journal of Instruction Level Parallelism (JILP)*, January 2005.
77. Glenn Reinman. Using an Operand File to Save Energy and to Decouple Commit Resources. In the *IEE Proceedings on Computers and Digital Techniques*, Vol 152, Issue 5, September 2005.
78. Glenn Reinman and Brad Calder. Using a Serial Cache for Energy Efficient Instruction Fetching. In the *Journal of Systems Architecture (JSA)*, 2004.
79. Brad Calder and Glenn Reinman. A Comparative Survey of Load Speculation Architectures. In the *Journal of Instruction Level Parallelism (JILP),* May 2000.
80. Glenn Reinman, Brad Calder, and Todd Austin. Optimizations Enabled by a Decoupled Front-End Architecture. *IEEE Transactions on Computing (TOC)*, Vol 50, No 4, February 2000.

Textbook Chapters:

81. Glenn Reinman. Chapter 2: Instruction Cache Prefetching. *Speculative Execution in High Performance Computer Architectures.* Edited by David Kaeli and Pen Yew. CRC Press, 2005.

Technical Reports:

82. Glenn Reinman and Norm Jouppi. CACTI version 2.0: An Integrated Cache Timing and Power Model. WRL Research Report, 2000/7.

Expert Witness Experience

Patent Infringement Cases:

1. **Sidley Austin LLP, 2011-Present**
   Has not started.
2. **Irell and Manella LLP, 2011-Present**
   Analysis of patents and technical specifications. Construction of claim charts. Software profiling.
3. **Irell and Manella LLP, 2011-Present**
   Analysis of patents and technical specifications. Construction of claim charts, drafted a declaration.
4. **Wilmer Hale LLP, 2011-Present**
   Analysis of patents and prior art.
5. **Irell and Manella LLP, 2009-2010**
   Analysis of patents and technical specifications. Implemented designs on simulation framework to analyze performance impact of various patents.
6. **Irell and Manella LLP, 2009**
   Analysis of patents and technical specifications.
7. **Simpson Thatcher & Bartlett LLP, 2008-2011**
   Analysis of patents and detailed technical specifications including a large repository of verilog source code. Wrote four detailed expert reports, and supporting statements for a number of motions. Was deposed for over a day and a half to testify about both infringement and invalidity of two asserted patents.
8. **Fish and Richardson LLP, 2008**
   Analysis of patents and technical specifications.
9. **Foley and Lardner LLP, 2007**
   Analysis of patents and technical specifications involving cache coherency and chip multiprocessors. Prepared an expert witness report after analyzing a significant amount of design drawings and microcode.
10. **Irell and Manella LLP, 2006**
    Analysis of patents and technical specifications.

Awards and Grants

- NSF Expedition Grant (CO-PI) to establish the *Center for Domain Specific Computing (CDSC)*, 8/2009-7/2014
  - Architecture Thrust Leader (one of four members of the Executive Committee for the Center)
- Semiconductor Research Corp 2008-HJ-1796 (PI) - *Network-On-Chip Design with RF-Interconnects for Future Chip Multiprocessors* – 4/2008-5/2011
- Best Paper Award, *International Symposium on High-Performance Computer Architecture*, Feb 2008.
- Voted Professor of the Year by the Engineering Society of the University of California, 2006
- UCLA Faculty Career Development Award 2004
- Northrop Grumman Excellence in Teaching Award 2004
- DARPA SA5430-79952 (CO-PI) - GSRC-MARCO, 9/2006-8/2007
- Semiconductor Research Corp 2005-TJ-1317 (CO-PI) - *Design and Evaluation of Power-Efficient High-Performance Heterogeneous Multi-Core Processors w/Programmable Fabric*, 6/2005-5/2008
- UC MICRO Program (CO-PI) – *MEVA: Microarchitectural Evaluation with Physical Planning*, 7/2003-12/2004
- NSF ITR (CO-PI) – *Reconfigurable Fabric*, 9/01/2002-8/31/2005
- NSF CAREER Award (PI) – *The Evaluation and Design of an Scalable, High-Performance, and Energy-Efficient Microprocessor Architecture*, 9/01/2001-8/31/2006

References

Available upon request.